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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/757,115	01/14/2004	Steven O. Smith	24317/82951	2949

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EXAMINER	
NGUYEN, HIEP	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 07/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/757,115	SMITH ET AL.	
	Examiner	Art Unit	
	Hiep Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 April 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *10-16* is/are allowed.

6)☒ Claim(s) *1 and 17* is/are rejected.

7)☒ Claim(s) *2-9 and 18-20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

The amendment filed on 04-21-2005 has been received and entered in the case. The arguments with respect to the reference of Memida are not deemed to be persuasive. Therefore, the rejections based on Memida's reference remain.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1 and 17 are rejected under 35 U.S.C. 102(b) as being anticipated by Memida (USP. 6,137,360).

Regarding claim 1, figure 13 of Memida shows a buffer comprising:

an input terminal (IN1) operable to receive an input signal;

an output terminal (OUT) at which an output signal for the buffer circuit is provided;

a first transistor (P101) having a gate, a source, and a drain, wherein the source of the first transistor is connected to the input terminal (IN1) via element (N111);

a second transistor (P102) having a gate, a source, and a drain, wherein the gate of the second transistor is connected to its drain and to the gate of the first transistor;

a third transistor (P131) having a gate, a source, and a drain, wherein the gate of the third transistor is connected to the drain of the first transistor (P101), wherein the source of the third transistor (P131) is connected to the output terminal and to the source of the second transistor (P102) via element (N112) and means for balancing the first transistor and the second transistor (feedback transistor N112) when a change occurs in the input signal appearing at the input terminal (col. 1, lines 64-76, col.3 lines 1-31).

Regarding claim 17, figure 13 of Memida shows a buffer circuit comprising:

an input terminal (IN1) operable to receive an input signal;

an output terminal (OUT) at which an output signal for the buffer circuit is provided;

at most three transistors (P101, P102, P131) operable to provide signal currents, wherein two of the three transistors are matched (P101, P102); and

means for feeding back (N112) the output signal so that the two matched transistors (P101, P102) are balanced in response to a change in the input signal appearing at the input terminal (col. 1, lines 64-76, col.3 lines 1-31).

Allowable Subject Matter

Claims 2-9 and 18-20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 10-16 are allowed.

Claims 2-9 and 18-20 are objected to because the prior art (USP. 6,137,360) fails to teach or fairly suggest a buffer comprising two current sources (fourth and fifth transistors) connected to the first and second transistors as called for in claims 2 and 7; a capacitor connected to the gate of the third transistor as called for in claim 9 and first and second current sources as called for in claim 18.

Claims 10-16 are allowed because the prior art (USP. 6,137,360) fails to teach or fairly suggest a buffer comprising first to sixth transistors as called for in claim 10.

Response to arguments

In the remarks, page 7, the Applicant argues that the input terminal IN1 in FIG. 13 of Memida is only connected to the gate of transistor M111 and no other part of the circuit, the input terminal IN1 is electrically isolated from transistor P101. In claim 1, the Applicant recites that "wherein the source of the first transistor is connected to the input terminal". In figure 13 of Memida is connected (or coupled) to the source of the first transistor (P101) via transistor (N111). Thus, the connection is similar to the connection recited in claim unless the Applicant recites a direct connection. The Applicant also argues that claim 17 recites a buffer comprising at most three transistors and Memida shows a buffer comprising five transistors.

Claim 17 reads on figure 1 of the present application and three transistors (16,28, 24) are part of a bigger circuit. Similarly, Memida shows a buffer comprising at most three transistors (P101, P102, P131). Transistors (N111) and (N112) are only means for connecting two of the at most three transistors (P101, P102, P131) to the rest of the bigger circuit. The similarity of the circuit of the present application and the circuit of Memida has been proven. The reference does not mention that the transistors in the circuit have different sizes thus, two transistors (P101) and (P102) are considered matched. Therefore, the rejection using Memida's circuit is proper.

Conclusion

Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Examiner Hiep Nguyen whose telephone number is (703) 305-0127. The examiner can normally be reached on Monday to Friday from 7:30 A.M.to 4:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached on (703) 308-4876. The fax phone number for this Group is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956.

Hiep Nguyen

06-07-05

TUAN T. LAM
PRIMARY EXAMINER